Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 62, 68, 71, 78, 84, and 91-95 as follows:

Listing of Claims:

1-61. (Cancelled)

62. (Currently Amended) A field emission display baseplate comprising:

a substrate having an upper surface;

a plurality of spaced-apart conductors formed on the substrate;

a plurality of spaced-apart emitter bodies comprising a high resistivity material formed on the conductors;

a porous silicon dioxide layer including respective openings coaxial with the emitter bodies, the porous silicon dioxide layer ~~formed on~~ disposed over and bonded to the upper surface of the substrate and the conductors, the porous silicon dioxide layer comprising about 22.5 to about 61.5 percent voids and a relative dielectric constant of less than three;

an extraction grid formed on the porous silicon dioxide layer and including respective openings coaxial with the emitter bodies; and

an emitter tip formed on each of the emitter bodies in the extraction grid opening, the tip formed from a material having a work function or electron affinity of less than four electron volts.

63. (Previously Presented) The baseplate of claim 62 wherein the porous silicon dioxide layer comprises at least 50% voids.

64. (Previously Presented) The baseplate of claim 62 wherein the porous silicon dioxide layer has a relative dielectric constant of less than 1.6.

65. (Previously Presented) The baseplate of claim 62 wherein the emitter tip comprises a material selected from a group consisting of: SiC, Zr, La, Zn, TiN, LaB_6, Ce, Ba, diamond and silicon oxycarbide.

66. (Previously Presented) The baseplate of claim 62 wherein the emitter body comprises:

silicon monoxide; and

a metal.

67. (Previously Presented) The baseplate of claim 62 wherein the emitter body comprises:

silicon monoxide; and

less than 10 atomic percent manganese.

68. (Currently Amended) A field emission display baseplate comprising:

a substrate having an upper surface;

a plurality of conductors formed on the substrate;

a plurality of emitters each formed on one of the plurality of conductors;

an oxidized porous polysilicon layer ~~formed on~~ disposed over and bonded to the upper surface of the substrate and the conductors;

an extraction grid formed on the oxidized porous polysilicon layer and including an opening;

an opening formed in the oxidized porous polysilicon layer coaxial with the opening in the extraction grid;

an emitter body comprising a high resistivity material formed in the opening in the oxidized porous polysilicon layer; and

an emitter tip formed on the emitter body and in the extraction grid opening, the tip formed from a material having a work function or electron affinity of less than four electron volts.

69. (Previously Presented) The baseplate of claim 68 wherein the oxidized porous polysilicon layer comprises about 22.5 to about 61.5 percent voids and a relative dielectric constant of less than three.

70. (Previously Presented) The baseplate of claim 68 wherein the oxidized porous polysilicon layer comprises about 22.5 to about 61.5 percent voids and a relative dielectric constant of less than 1.6.

71. (Currently Amended) A field emission display baseplate comprising:

a substrate having an upper surface;

a plurality of spaced-apart conductors formed on the substrate;

an oxidized porous polysilicon layer disposed over and bonded to ~~a~~ the upper surface of the substrate and ~~a surface of~~ the conductors;

an extraction grid formed on the oxidized porous polysilicon layer and including an opening;

an opening formed in the oxidized porous polysilicon layer coaxial with the opening in the extraction grid; and

an emitter formed in the opening in the oxidized porous polysilicon layer and in the extraction grid opening.

72. (Previously Presented) The baseplate of claim 71 wherein the oxidized porous polysilicon layer comprises about 22.5 to about 61.5 percent voids and a relative dielectric constant of less than three.

73. (Previously Presented) The baseplate of claim 71 wherein the oxidized porous polysilicon layer comprises about 22.5 to about 61.5 percent voids and a relative dielectric constant of less than 1.6.

74. (Previously Presented) The baseplate of claim 71 wherein emitter comprises:

an emitter body comprising a high resistivity material; and

an emitter tip formed on the emitter body and in the extraction grid opening.

75. (Previously Presented) The baseplate of claim 74 wherein the emitter tip comprises a material selected from a group consisting of: SiC, Zr, La, Zn, TiN, LaB_6, Ce, Ba, diamond and silicon oxycarbide.

76. (Previously Presented) The baseplate of claim 74 wherein the emitter body comprises:

silicon monoxide; and

a metal.

77. (Previously Presented) The baseplate of claim 74 wherein the emitter body comprises:

silicon monoxide; and

less than 10 atomic percent manganese.

78. (Currently Amended) A field emission display comprising:

a substrate having an upper surface;

a plurality of emitters formed on the substrate, each of the emitters being formed on a conductor;

a porous silicon dioxide layer ~~formed on~~ disposed over and bonded to the upper surface of the substrate and the conductors, the porous silicon dioxide layer comprising about 22.5 to about 61.5 percent voids and a relative dielectric constant of less than three, the porous silicon dioxide layer including respective openings formed about each of the emitters;

an extraction grid extraction grid formed substantially in a plane defined by respective tips of the plurality of emitters and having an opening surrounding each tip of a respective one of the emitters; and

a cathodoluminescent-coated faceplate having a planar surface formed parallel to and near the plane of tips of the plurality of emitters.

79. (Previously Presented) The display of claim 78 wherein the porous silicon dioxide layer comprises at least 50% voids.

80. (Previously Presented) The display of claim 78 wherein the porous silicon dioxide layer has a relative dielectric constant of less than 1.6.

81. (Previously Presented) The display of claim 78 wherein each of the emitters comprise:

an emitter body comprising a high resistivity material; and

an emitter tip formed on the emitter body and in the extraction grid opening.

82. (Previously Presented) The display of claim 81 wherein:

the emitter tips each comprise a material selected from a group consisting of: SiC, Zr, La, Zn, TiN, LaB_6, Ce, Ba, diamond and silicon oxycarbide; and

the emitter bodies each comprise a cermet material.

83. (Previously Presented) The baseplate of claim 81 wherein the emitter bodies each comprise:

silicon monoxide; and

less than 10 atomic percent metal.

84. (Currently Amended) A computer system comprising:

a central processing unit;

a memory device coupled to the central processing unit, the memory device storing instructions and data for use by the central processing unit;

an input interface; and

a display, the display comprising:

a cathodoluminescent layer formed on a conductive surface of a transparent faceplate;

a substrate having an upper surface, the substrate disposed substantially parallel to and near the cathodoluminescent layer formed on the faceplate;

a plurality of conductors formed on the substrate;

a plurality of emitters formed on the conductors;

a porous silicon dioxide layer including respective openings formed about each of the emitter bodies, the porous silicon dioxide layer ~~formed on~~ disposed over and bonded to the upper surface of the substrate and the conductors, the porous silicon dioxide layer comprising about 22.5 to about 61.5 percent voids and a relative dielectric constant of less than three; and

an extraction grid formed on the porous silicon dioxide layer and including openings each coaxial with one of the openings in the porous silicon dioxide layer.

85. (Previously Presented) The computer system of claim 84 wherein the porous silicon dioxide layer has a relative dielectric constant of less than 1.6.

86. (Previously Presented) The computer system of claim 84 wherein the porous silicon dioxide layer comprises at least 50% voids.

87. (Previously Presented) The computer system of claim 84 wherein each of the emitters comprises:

an emitter body comprising a high resistivity material; and

an emitter tip formed on the emitter body and in the extraction grid opening.

88. (Previously Presented) The computer system of claim 87 wherein:

the emitter tips each comprise a material selected from a group consisting of: SiC, Zr, La, Zn, TiN, LaB_6, Ce, Ba, diamond and silicon oxycarbide; and

the emitter bodies each comprise a cermet material.

89. (Previously Presented) The computer system of claim 87 wherein the emitter bodies each comprise:

silicon monoxide; and

less than 10 atomic percent metal.

90. (Previously Presented) The computer system of claim 87 wherein tips of the emitters are formed from materials having a work function of less than four electron volts.

91. (Currently Amended) The baseplate of claim 62 wherein the porous silicon dioxide layer has a mechanically planarized upper surface and wherein the extraction grid is formed on the mechanically planarized upper surface of the porous silicon dioxide layer.

92. (Currently Amended) The baseplate of claim 68 wherein the oxidized porous polysilicon layer has a mechanically planarized upper surface and wherein the extraction grid is formed on the mechanically planarized upper surface of the oxidized porous polysilicon layer.

93. (Currently Amended) The baseplate of claim 71 wherein the oxidized porous polysilicon layer has a mechanically planarized upper surface and wherein the extraction grid is formed on the mechanically planarized upper surface of the oxidized porous polysilicon layer.

94. (Currently Amended) The baseplate of claim 78 wherein the porous silicon dioxide layer has a mechanically planarized upper surface.

95. (Currently Amended) The baseplate of claim 84 wherein the porous silicon dioxide layer has a planarized upper surface and wherein the extraction grid is formed on the mechanically planarized upper surface of the porous silicon dioxide layer.